図1. R5～R0（全体）

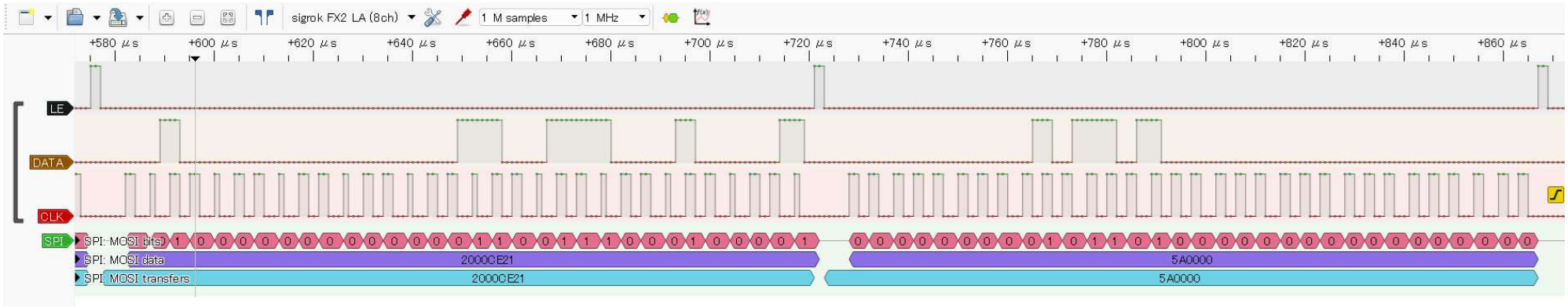

図2. R1～R0

DB	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
				12bit Fractional=0												16bit INT=180																INT
R0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	1	0	0	0	0	0	0	0	0	0
				0				0				0				0				A				5				0				0
				12bit Modulus=2500												12bit Phase=1																CPL/CPT		CPOC
R1	1	0	0	0	0	1	0	0	0	1	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
				1				2				E				C				0				0				0				2
				RST	TRI	HDN	PDP	LDP	LDF		CP=5mA			EG4	D					R counter=1							RDIV2	DBR		MUX		SDN	LDS
R2	0	1	0	0	0	0	1	1	0	1	1	1	1	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0
				2				C				E				9				0				0				1				1
				12bit CDIV=0												CDM		FUO				FUO			RET	SSH	I			VCO			
R3	1	1	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
				3				8				2				0				0				0				0				0
				APWR		RFA		BPWR		RFB	BDI	FUO				BS						DIVA			FB	BS			DREF	DDIV	SD	FUO	FUO
R4	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1	1	0	0	0	1	1	0
				C				F				1				0				2				8				3				6
				FUO															MX3	FUO		FUO		LD		F01			FUO			FUO
R5	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	0	0
				5				0				0				0				4				4				1				0
				V						FUO												ADC		POR				FUO				
R6	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
				6				0				0				0				0				0				0				0

表1. レジスター

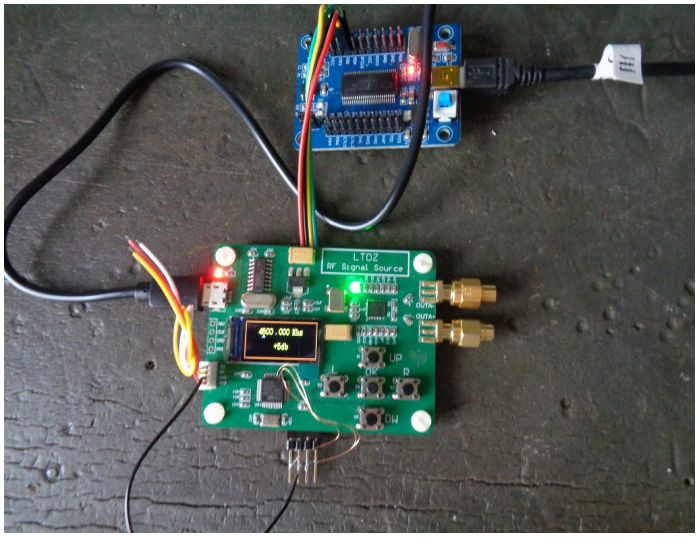

写真1. MAX2870基板